Deductive Temporal Verification of Parametrized Concurrent Systems

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Verification of Concurrent Data-structures

Main Idea

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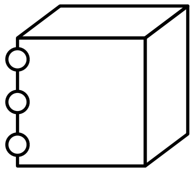
Concurrent DataStructure



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Most General Client

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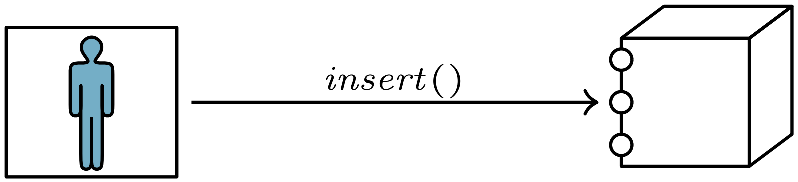

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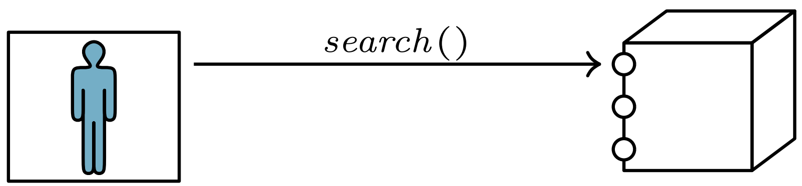

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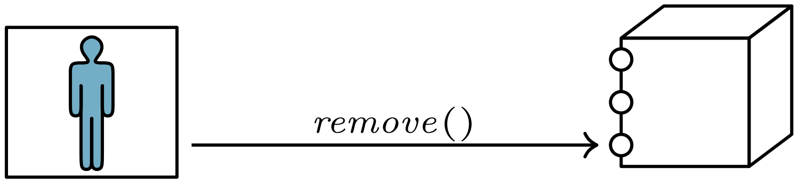

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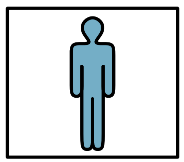

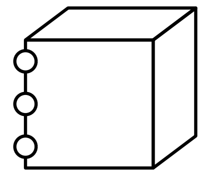

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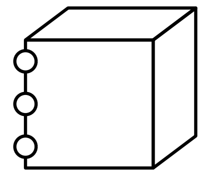

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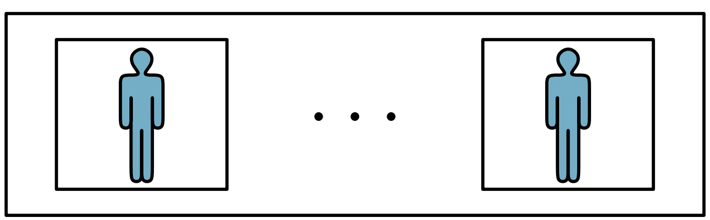

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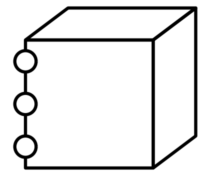

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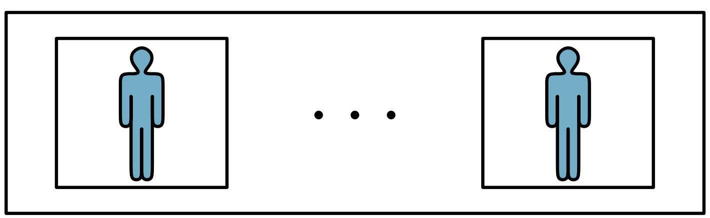

$$P[N] : P(1) || \cdots || P(N)$$

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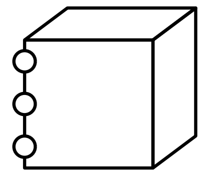

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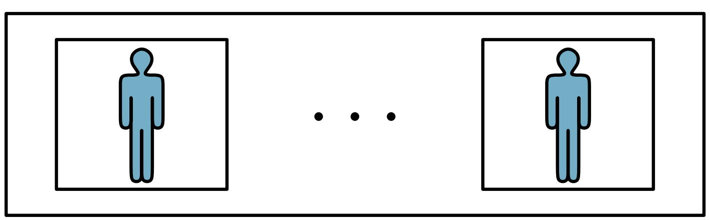

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Property

$$\varphi^{(k)}$$

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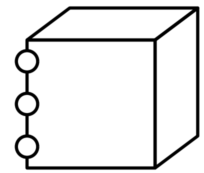

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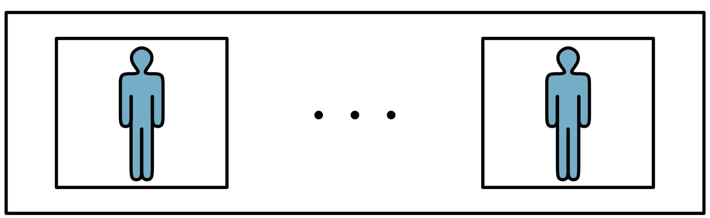

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LTL ($\Box$,$\Diamond$,$\mathcal{U}$,...)

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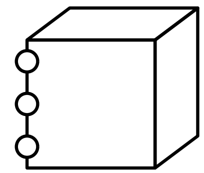

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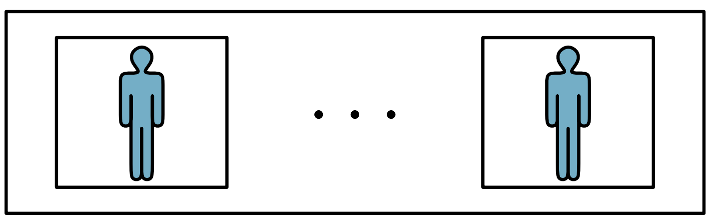

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Diagram

$\mathcal{D}$

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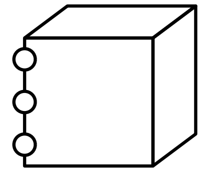

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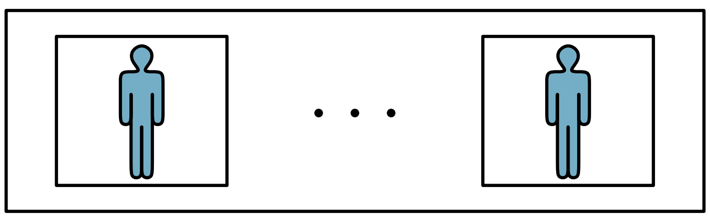

$P[N] : P(1)||\cdots||P(N)$

Diagram

Property

$\models \quad \mathcal{D} \quad \models \quad \varphi^{(k)}$

Verification Conditions:

- Initiation
- Consecution
- Acceptance
- Fairness

Satisfaction (Model Checking)

Motivating Example: Mutual Exclusion Algorithm

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global
  $\mathit{Int}\ \mathit{tick} := 0$
  $\mathit{Set}\langle \mathit{Int}\rangle\ \mathit{announced} := \emptyset$

procedure $\textsc{MutExc}$
  $\mathit{Int}\ \mathit{ticket}$
begin
loop
  nondet
    $\left\langle \begin{array}{l} \mathit{ticket} := \mathit{tick}++ \\ \mathit{announced}.\mathit{add}(\mathit{ticket}) \end{array} \right\rangle$
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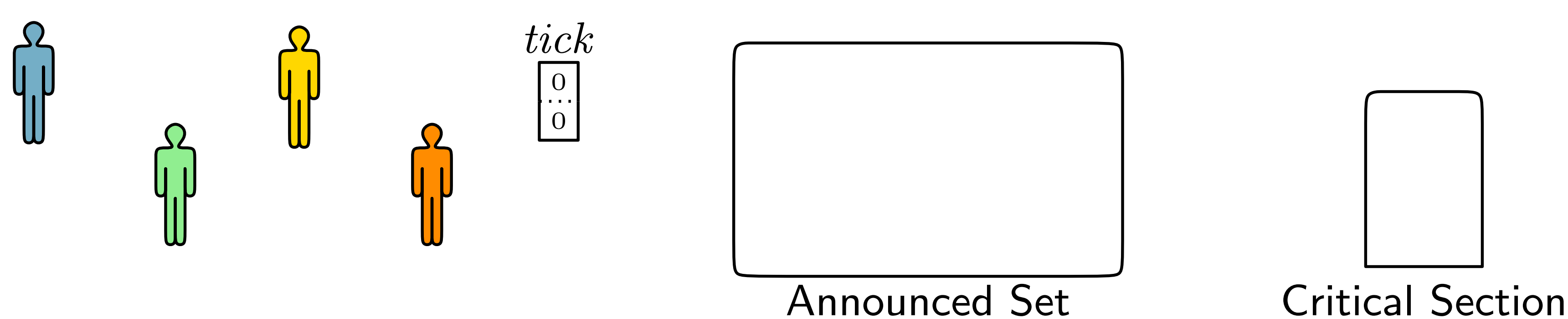

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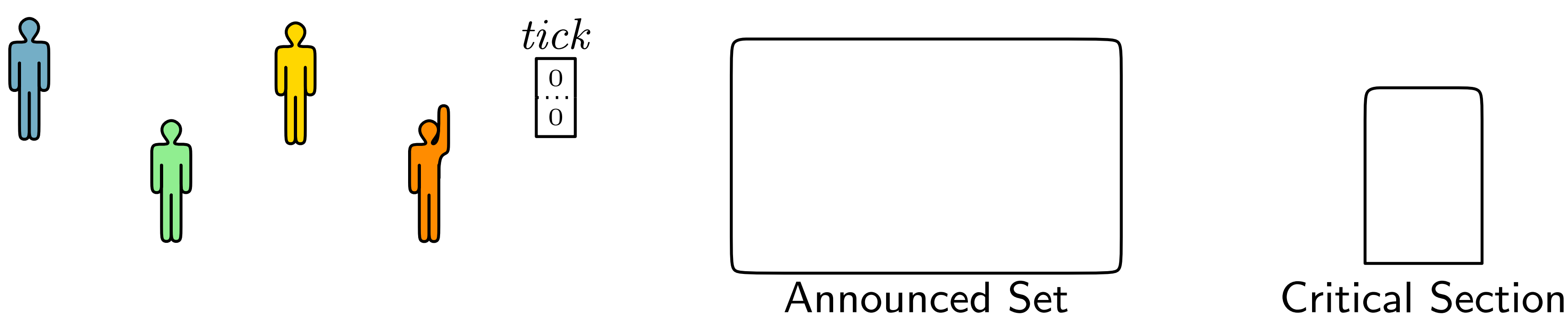

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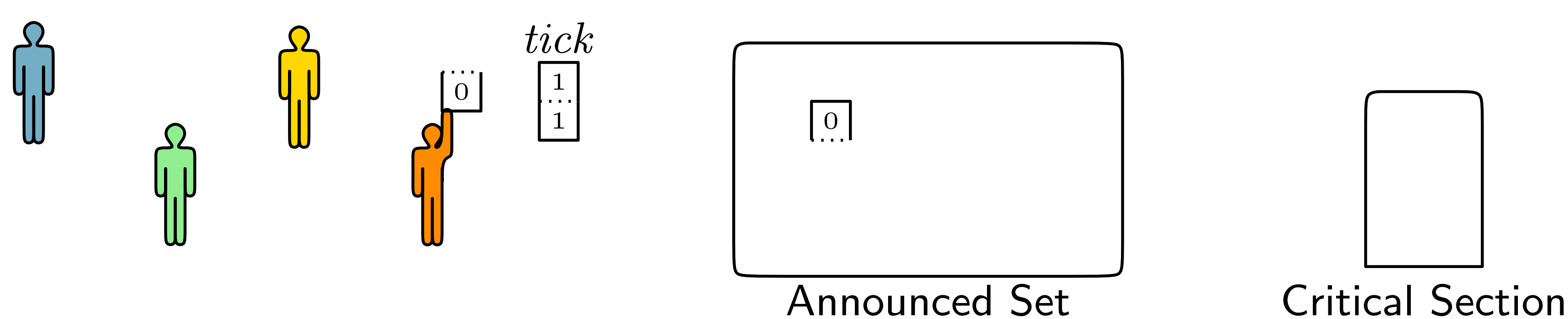

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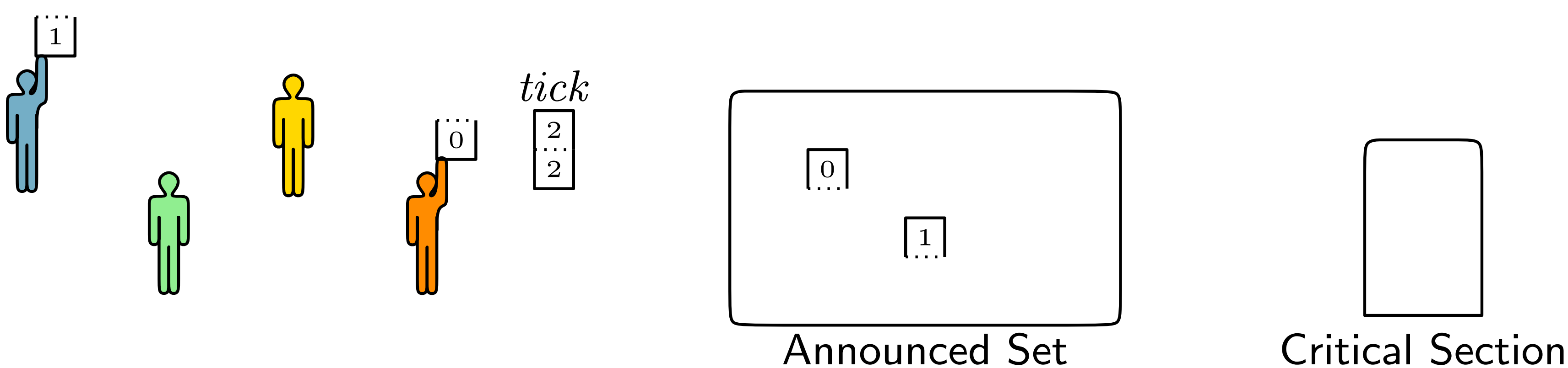

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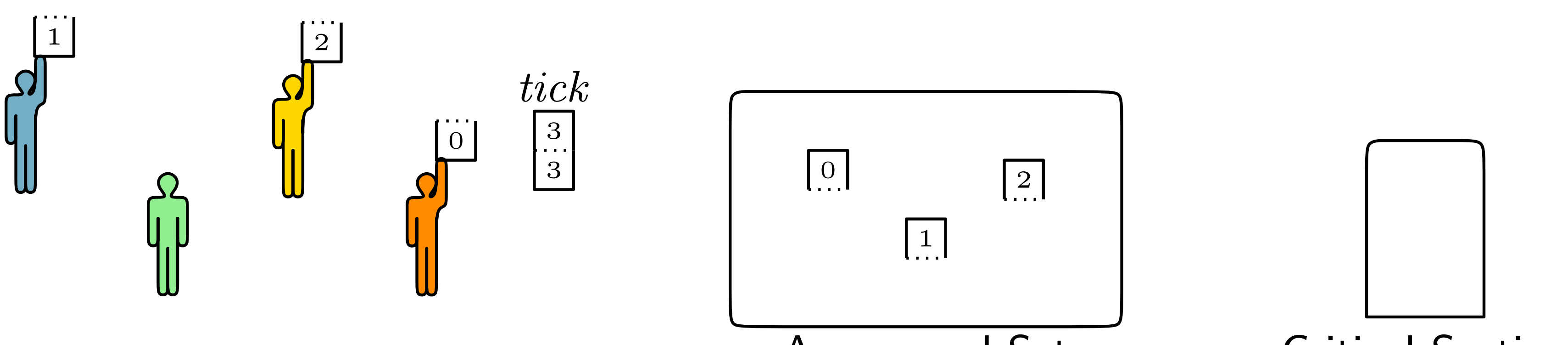

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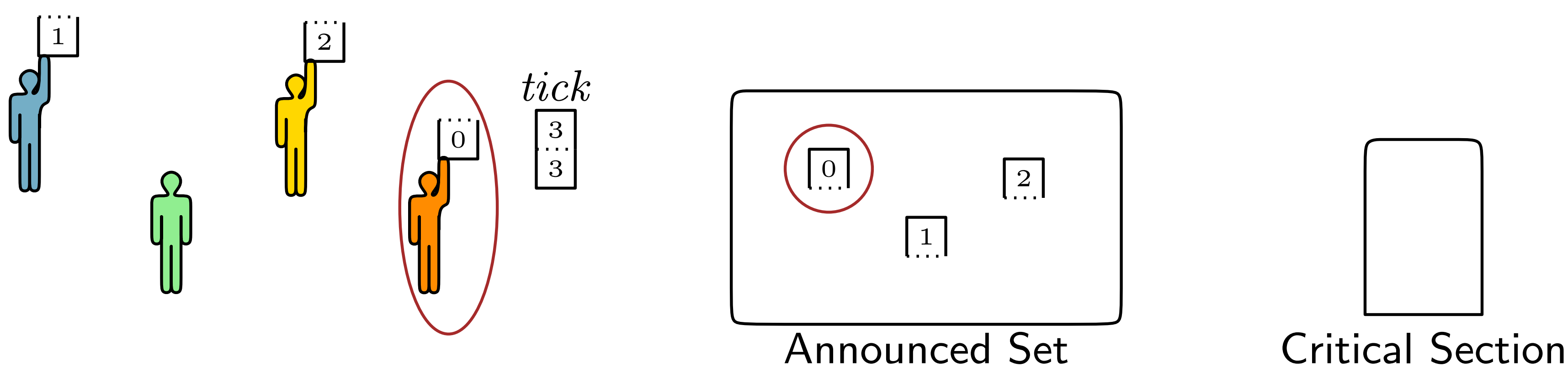

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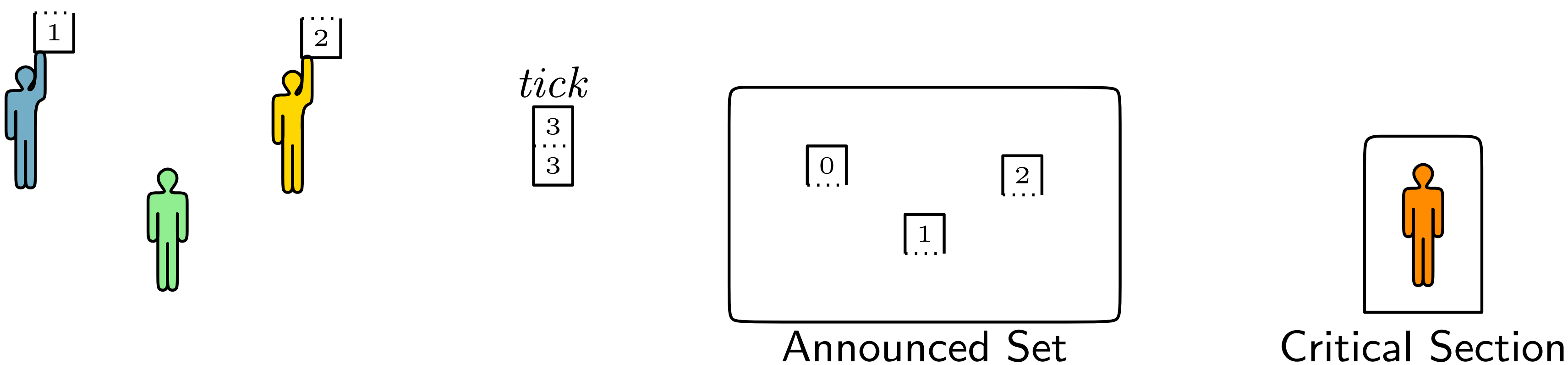

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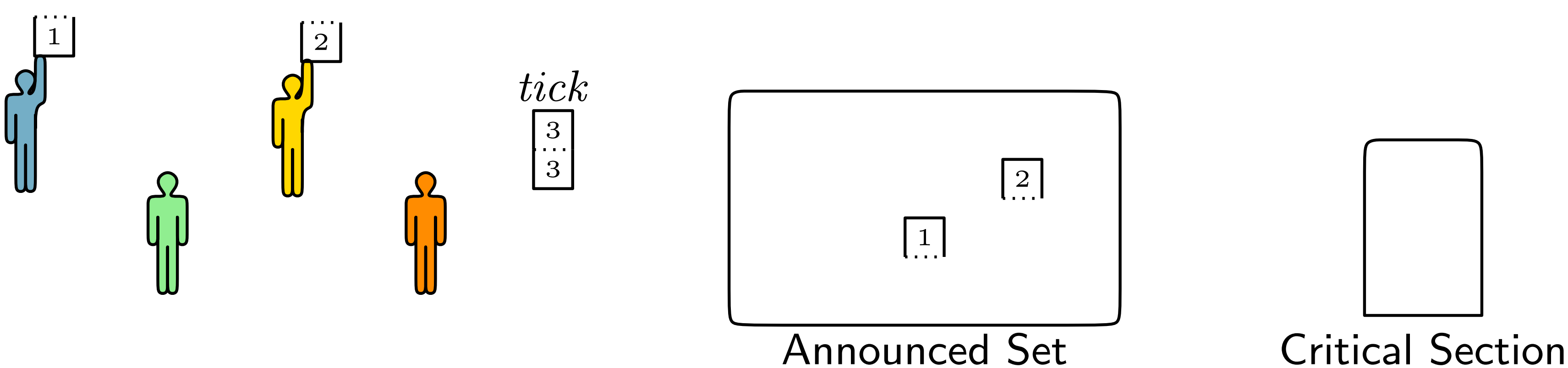

Verification Diagram for Mutual Exclusion Algorithm

- For all k, $\varphi(k) = \Box(announced(k) \to \Diamond access\_critical(k))$

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T_1 not interested

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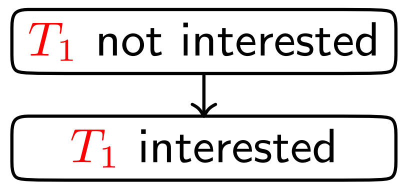

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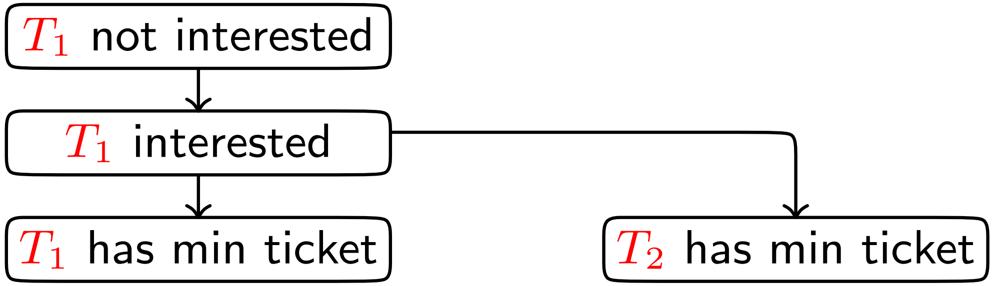

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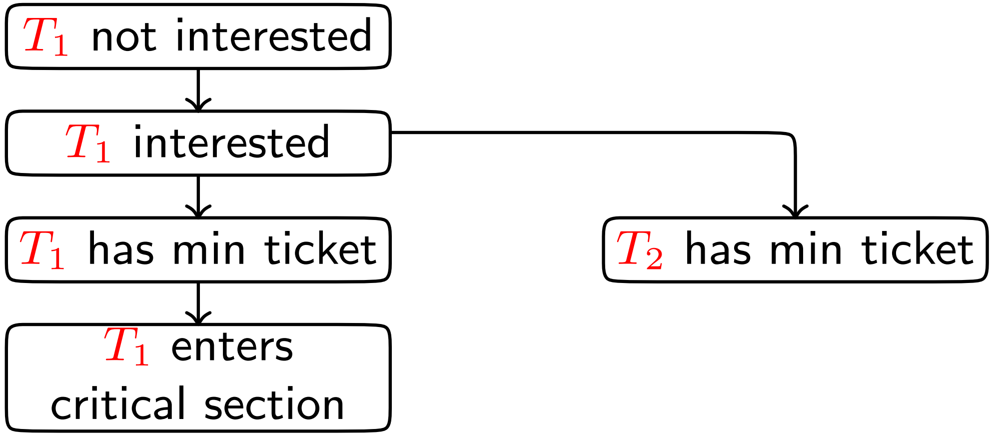

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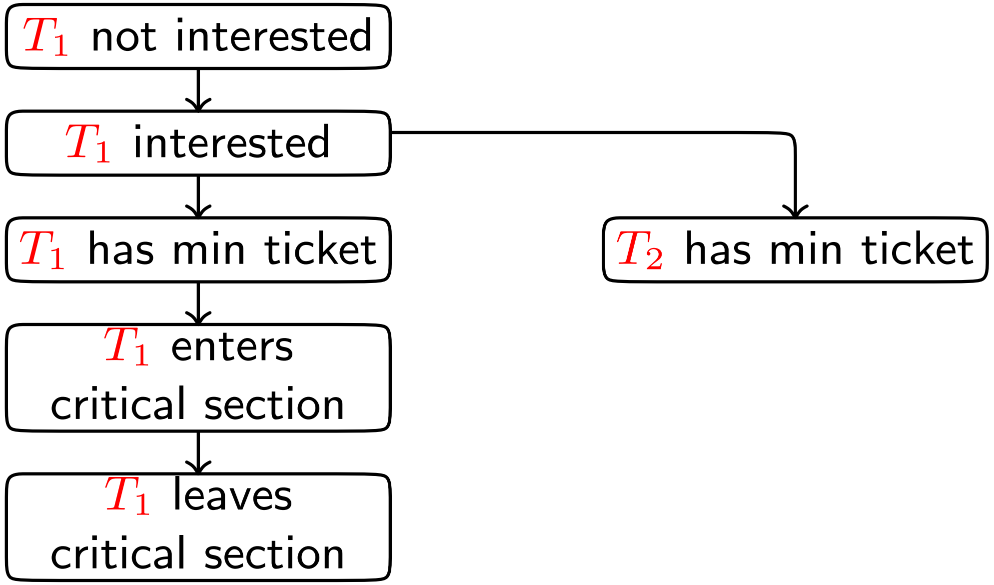

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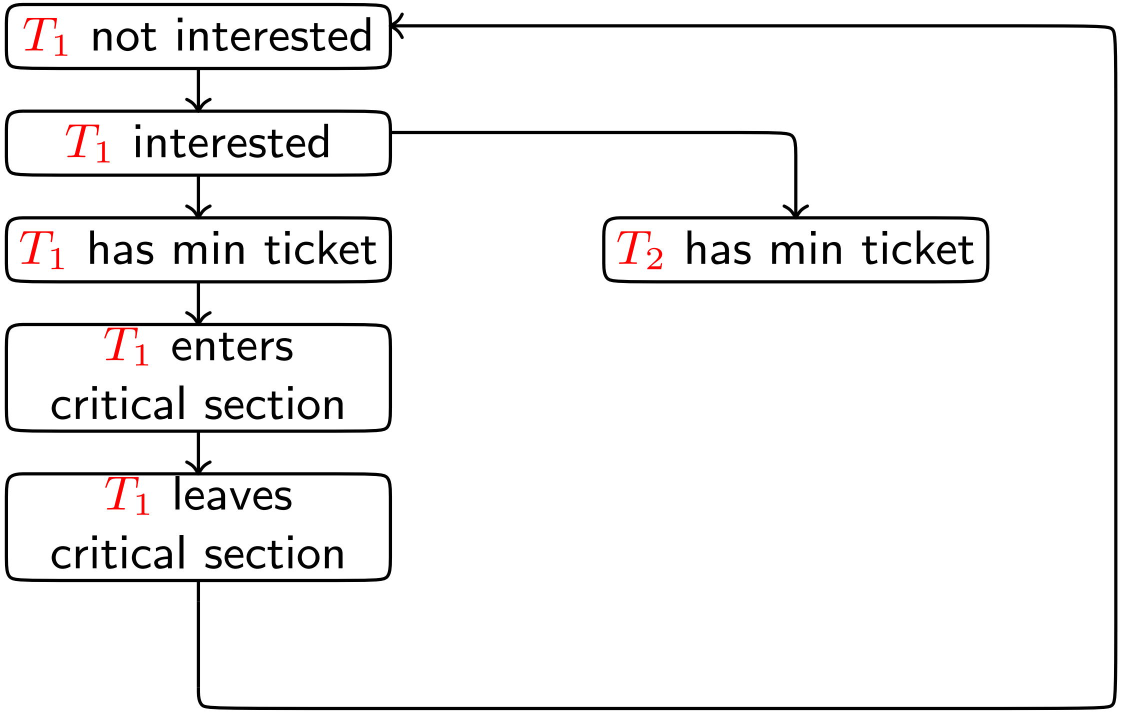

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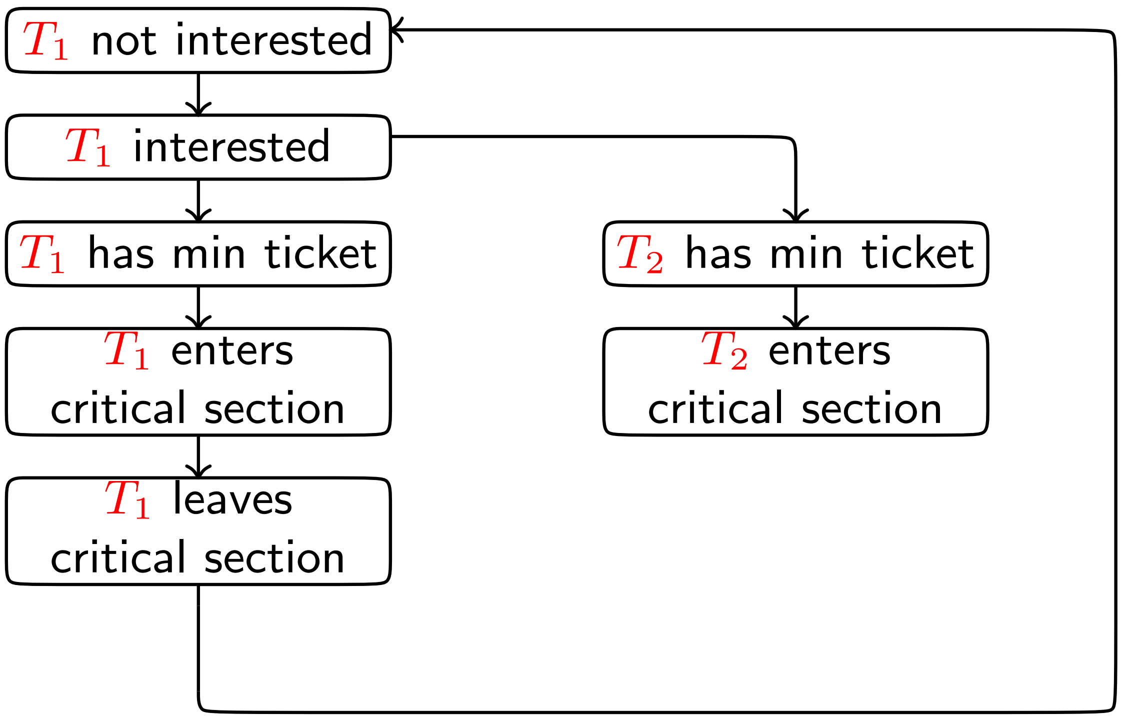

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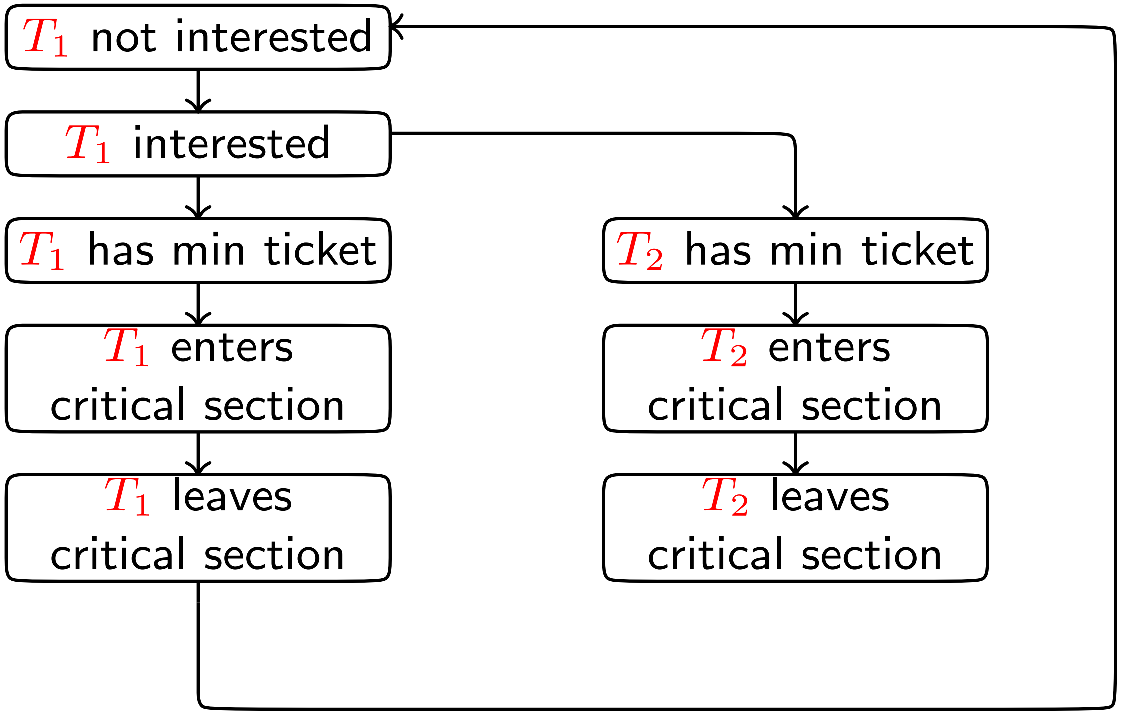

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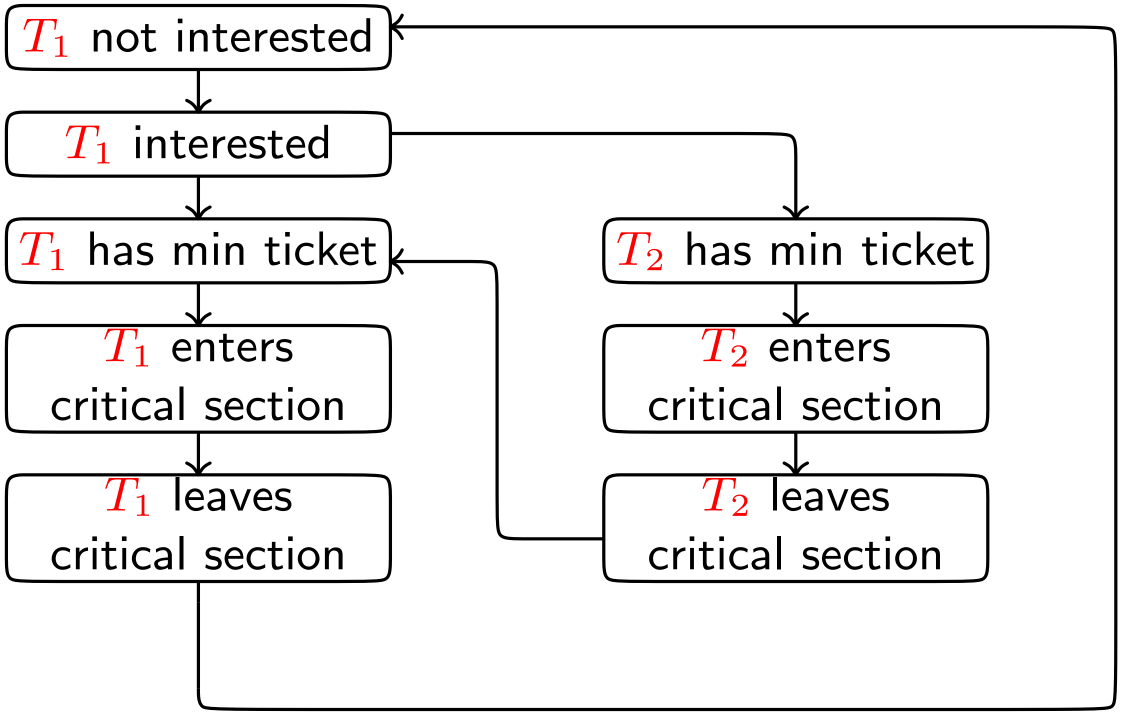

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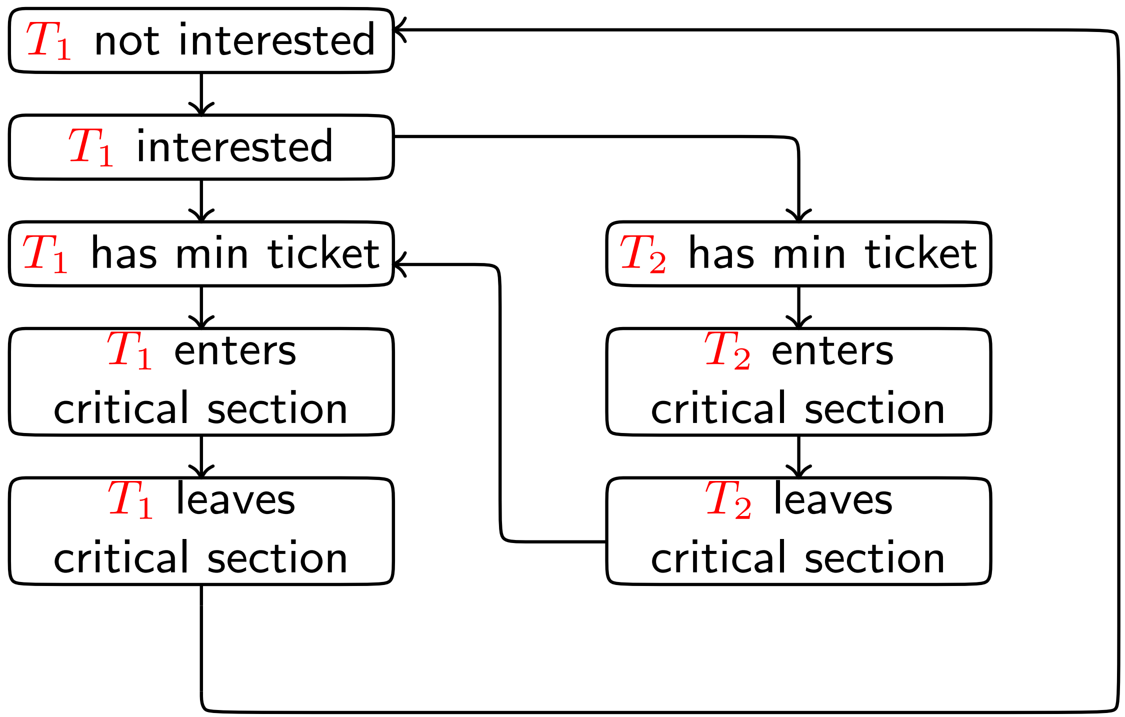

Some verification conditions

$$\left\{ \begin{array}{l} n \wedge \tau[1] \ \to \ succ(n) \\ n \wedge \tau[2] \ \to \ succ(n) \end{array} \right.$$

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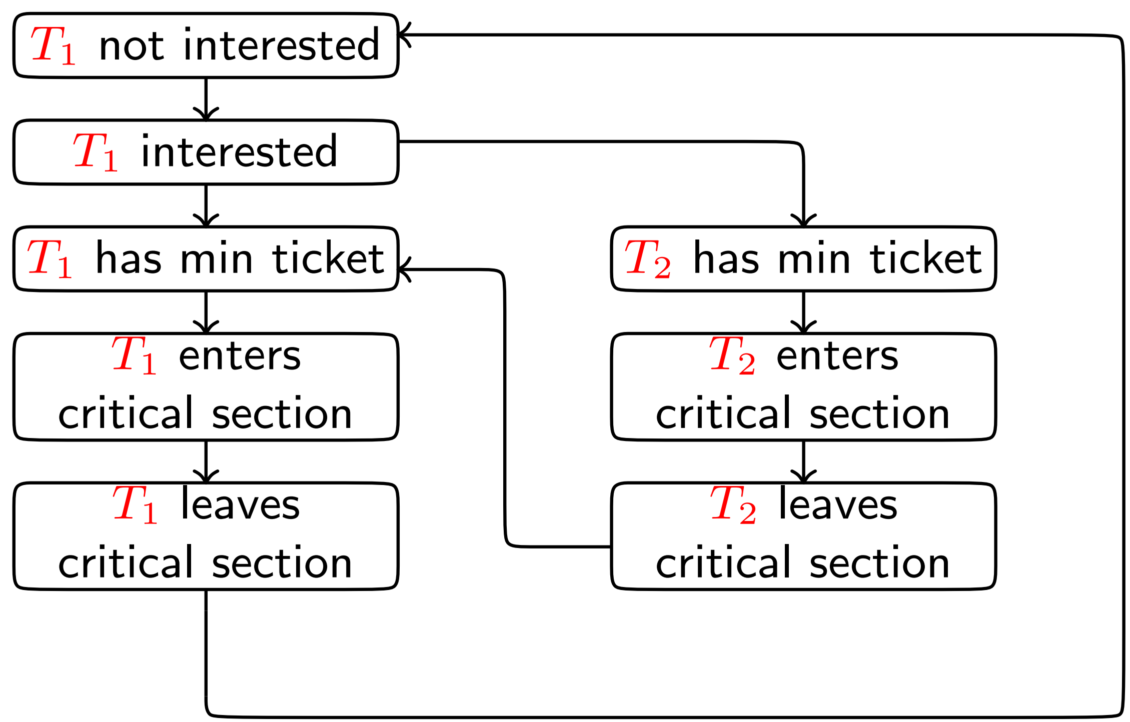
- Imagine now a system with 3 threads: T_1, T_2 and T_3



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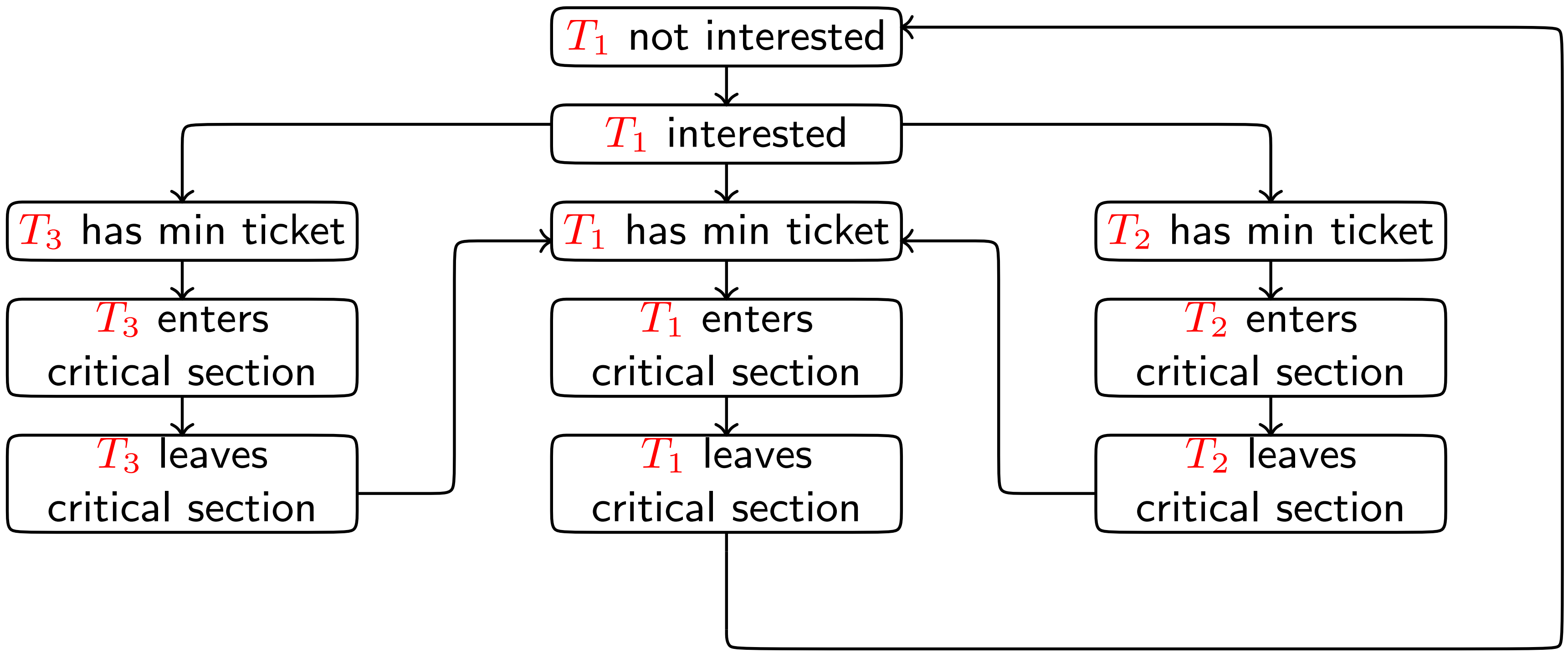

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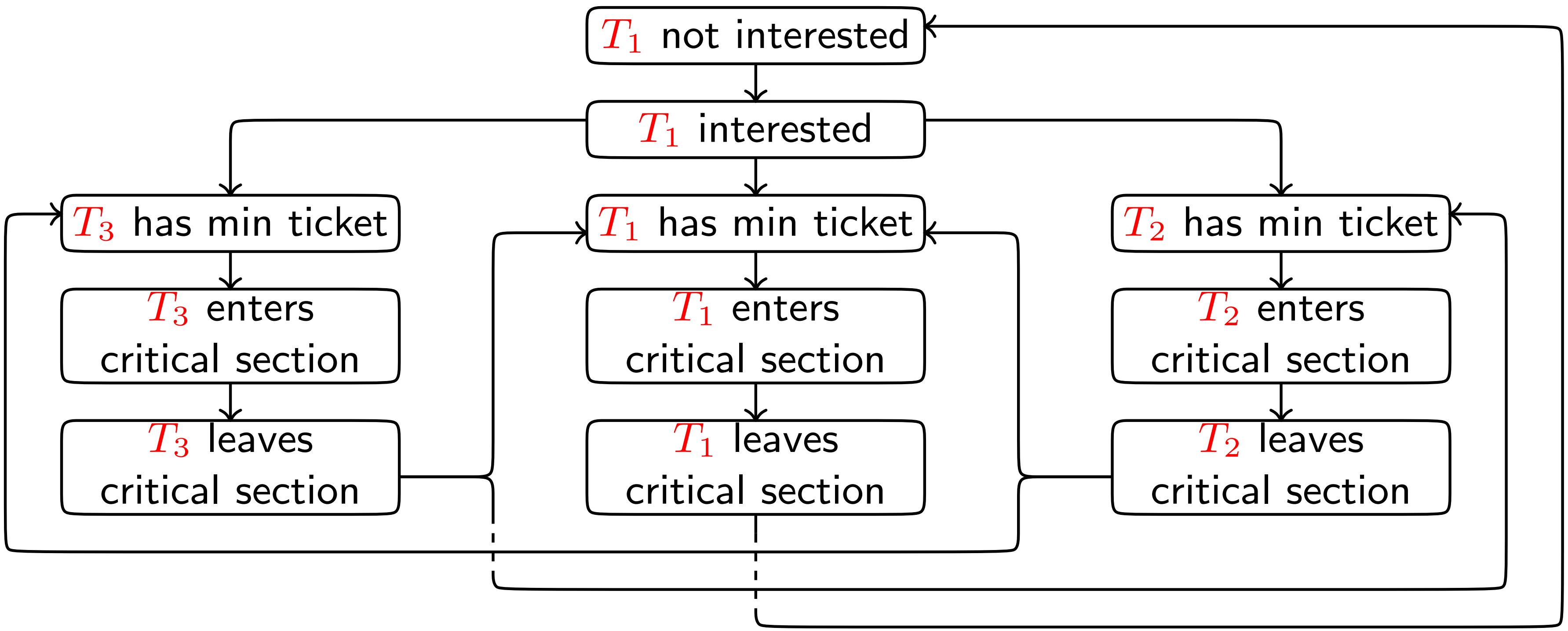

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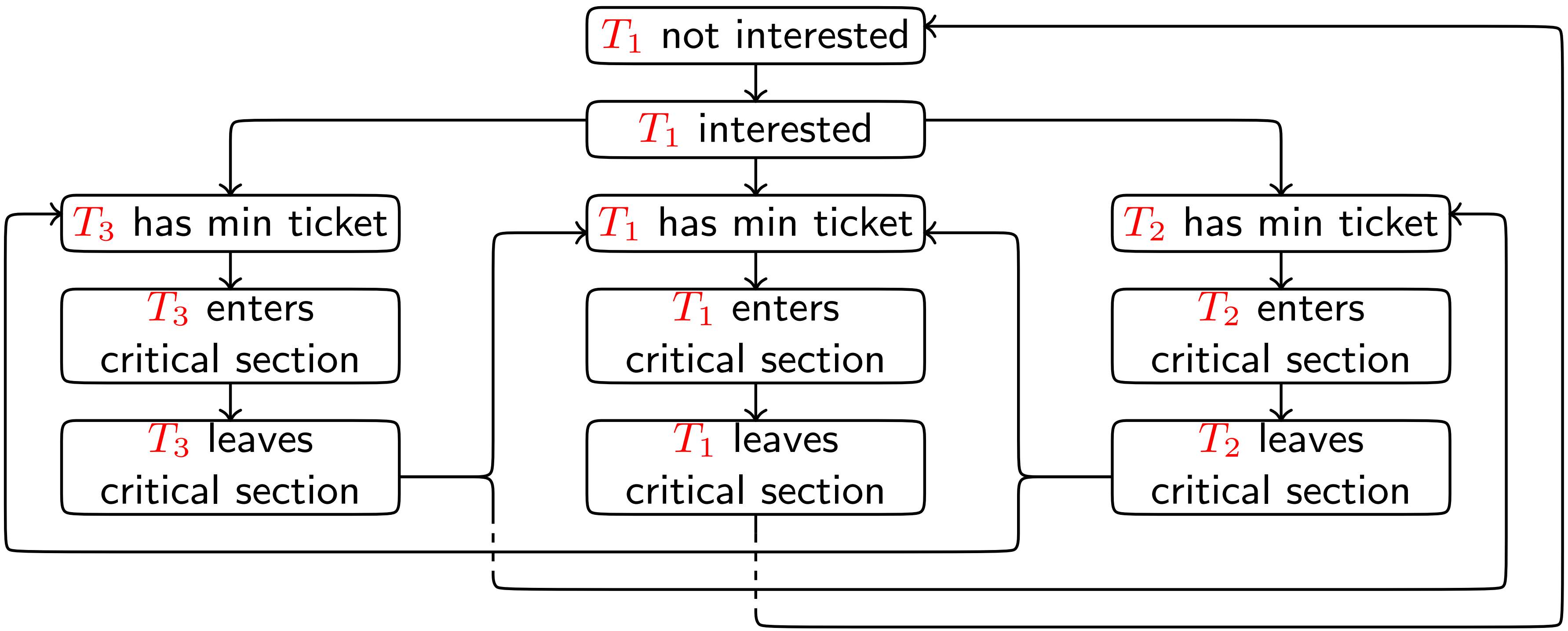

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Motivation for Parametrized Verification Diagrams

Problem

- **Not a single diagram** for arbitrary number of threads
- **Unbounded** number of **verification conditions**

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Problem

- **Not a single diagram** for arbitrary number of threads
- **Unbounded** number of **verification conditions**

Our solution

- **Unique diagram** for arbitrary number of threads
- **Finite and bounded** number of verification conditions

Parametrized Verification Diagrams exploits the similarities within **symetric systems**

Parametrized Fair Transition Systems

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- Let P be a program consisting of L **lines of code**

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$$\boxed{\mathcal{S}^{[M]} = \langle V, \Theta, \mathcal{T}, \mathcal{J} \rangle}$$

Parametrized Fair Transition Systems

- Let P be a program consisting of L **lines of code**
- Assuming M **threads** running program P
- Let V_{global} be the set of **global variables** of program P

$$\boxed{\mathcal{S}^{[M]} = \langle V, \Theta, \mathcal{T}, \mathcal{J} \rangle}$$

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procedure MutExc
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begin
loop
      nondet
      ⟨ ticket := tick++
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      await (announced.min == ticket)
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global
$\quad Int\ tick := 0$
$\quad Set\langle Int\rangle\ announced := \emptyset$

procedure $\textsc{MutExc}$
$\quad \boxed{Int\ ticket}$
begin
loop
$\quad$ **nondet**
$\quad \left\langle \begin{array}{l} ticket := tick{+}{+} \\ announced.add(ticket) \end{array} \right\rangle$
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\begin{aligned}
V &= \{tick, announced\} \cup \\
&\quad \{ticket[1], ticket[2]\} \cup \\
&\quad \{pc[1], pc[2]\} \\
\mathcal{T} &= \bigcup_{l \in 1..7} \{\tau_l[1], \tau_l[2]\} \\
\mathcal{J} &= \mathcal{T}
\end{aligned}
$$

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- Assume a parametrized transition system $\mathcal{S}^{[M]}$
- All threads execute the **same program**
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$$
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& s_0^{i \leftrightarrow j} & s_1^{i \leftrightarrow j} & s_2^{i \leftrightarrow j} & \dots
\end{tikzcd}
$$

$i, j \in [M]$ | switch $v[i]$ with $v[j]$

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\downarrow & & \downarrow & & \downarrow & & \downarrow & & \\
\sigma^{i\leftrightarrow j} & = & s_0^{i\leftrightarrow j} & \xrightarrow{\tau_0^{i\leftrightarrow j}} & s_1^{i\leftrightarrow j} & \xrightarrow{\tau_1^{i\leftrightarrow j}} & s_2^{i\leftrightarrow j} & \xrightarrow{\tau_2^{i\leftrightarrow j}} & \dots
\end{array}$$

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- For each $v : \alpha$, we add $f_v : \mathsf{tid} \rightarrow \alpha$

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  - stable infinite $\xrightarrow{\textbf{combinable with}}$ stable infinite theories
  - polite $\longrightarrow$ non stable infinite theories

$$\boxed{T = T_{\mathsf{prog}} + T_{\mathsf{param}}}$$

Soundness of Parametrized Verification Diagrams

Theorem:

Let $\mathcal{S}^{[M]}$ be a symmetric parametrized FTS and $\varphi(k)$ a temporal formula.

If there exists a (M,k)-valid PVD $\mathcal{D}^{[M]}$, then:

$$\boxed{\mathcal{S}^{[M]} \qquad \models \qquad \varphi(k)}$$

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$$\boxed{\mathcal{S}^{[M]} \ \models\ \mathcal{D}^{[\mathcal{M}]} \ \models\ \varphi(k)}$$

for all M

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a

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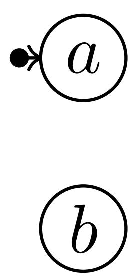

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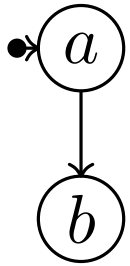

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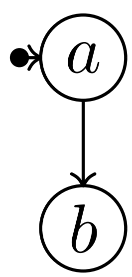

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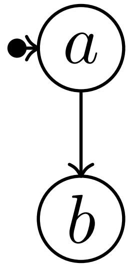

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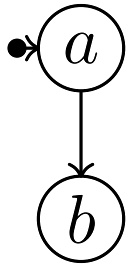

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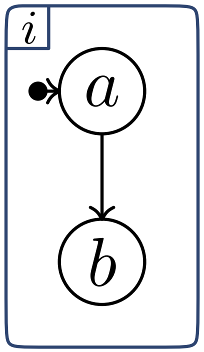

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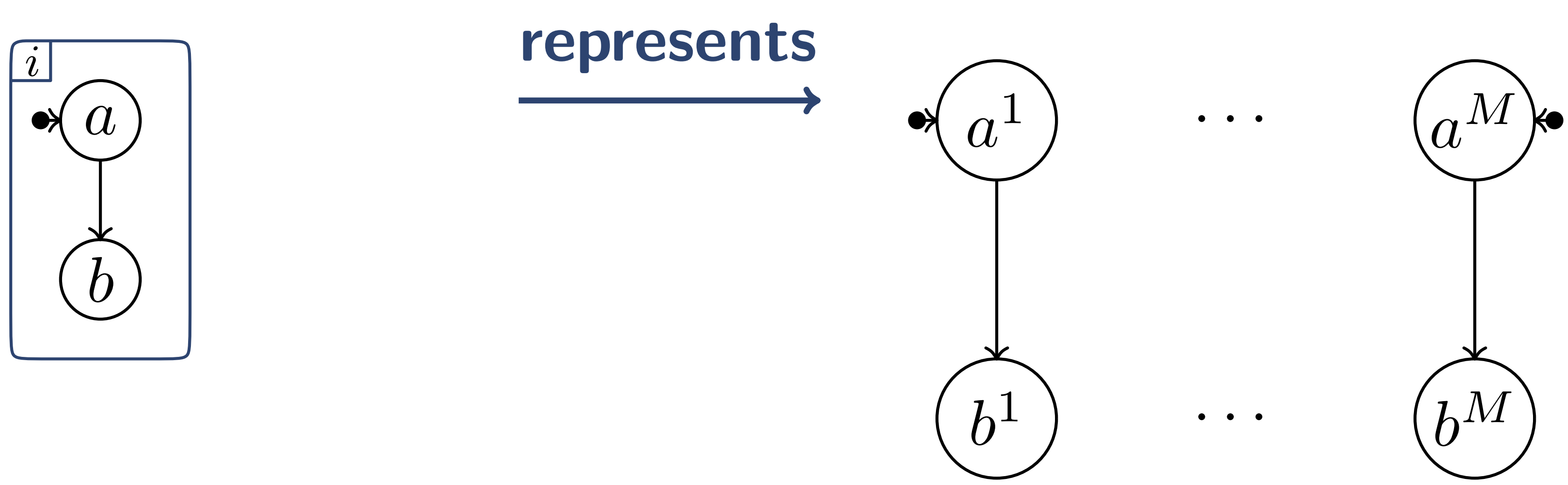
For M threads



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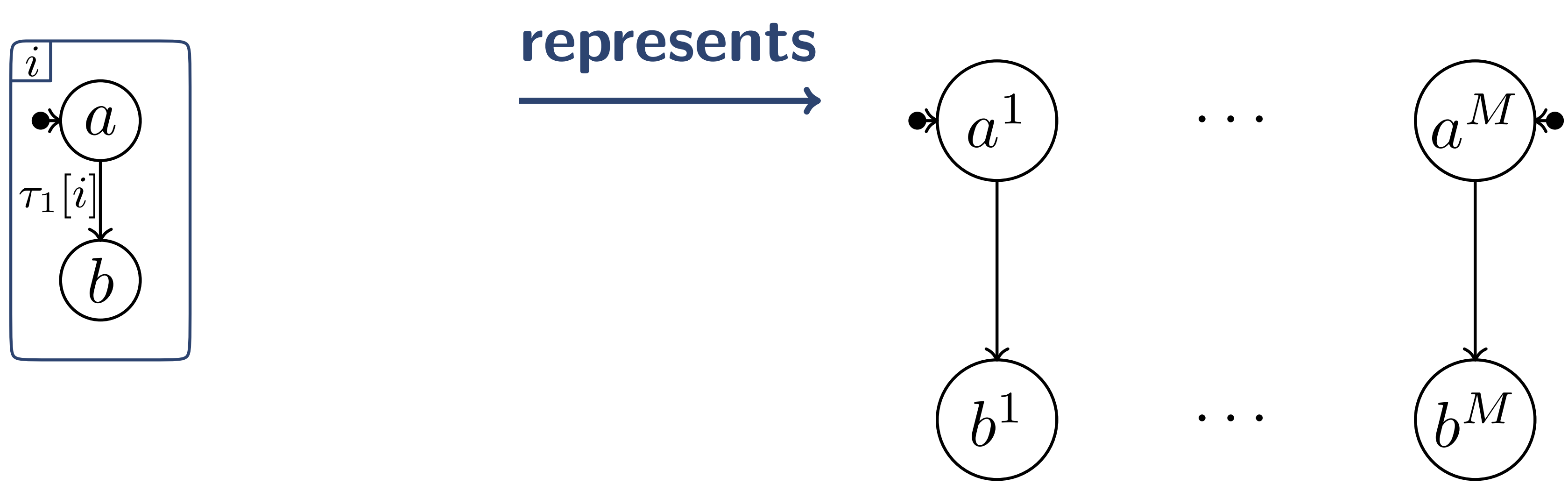

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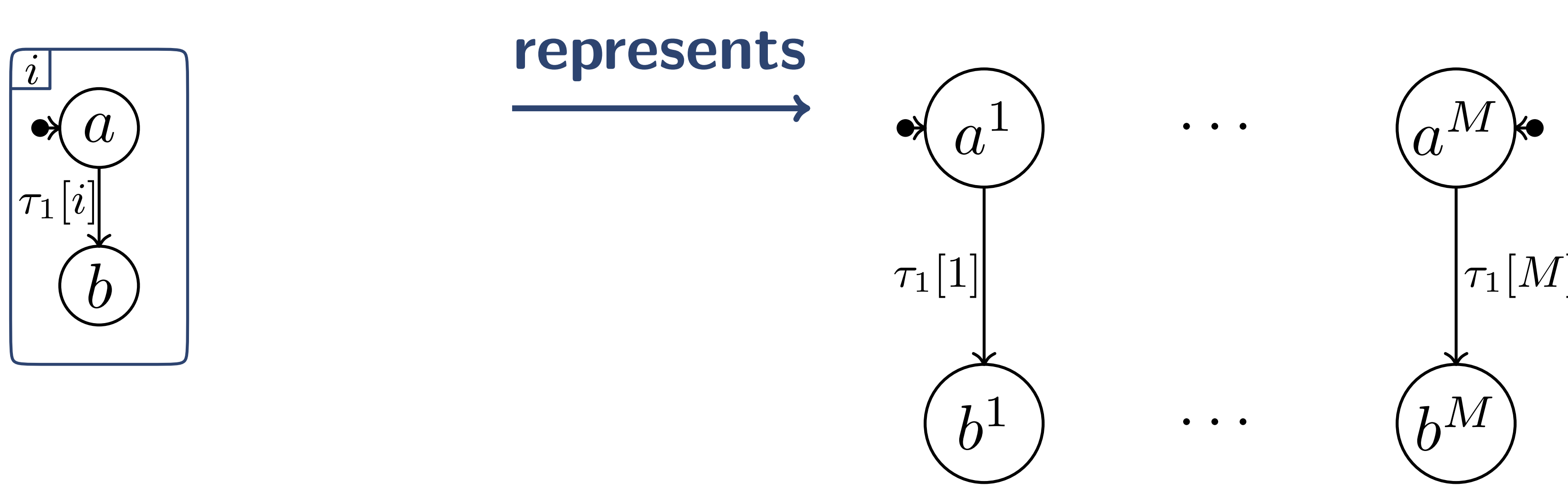

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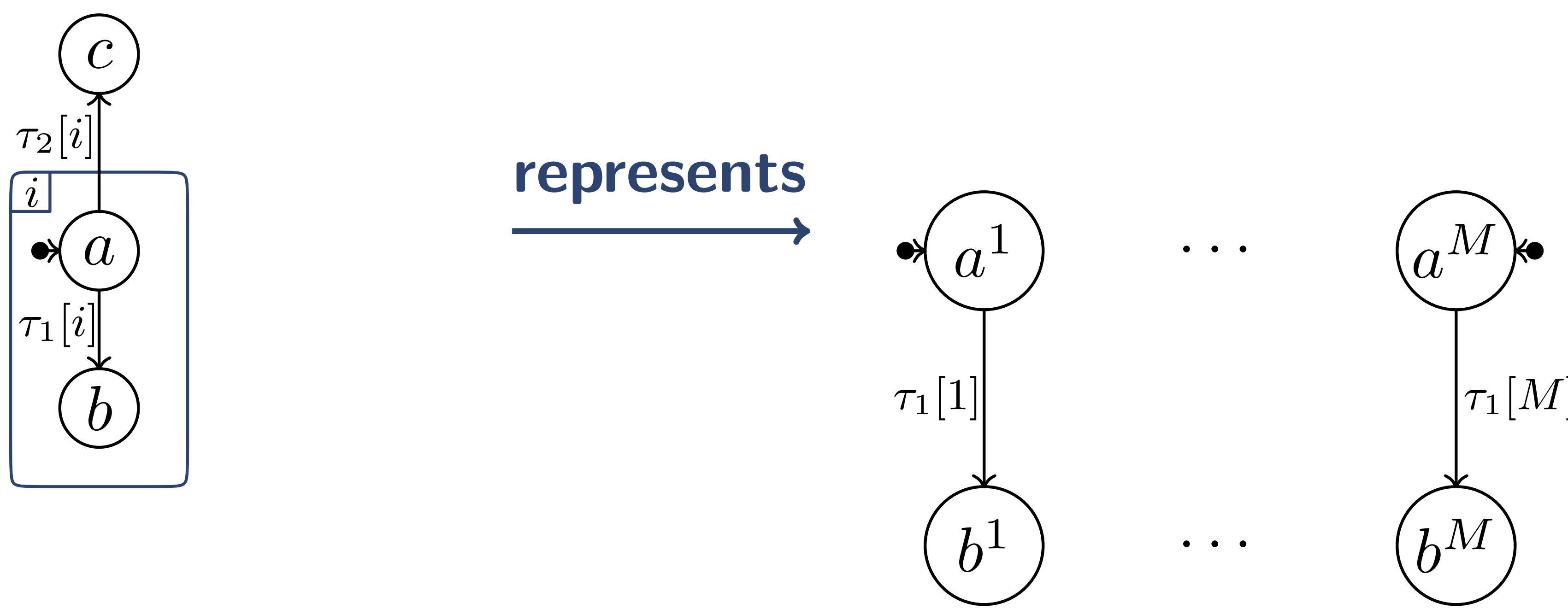

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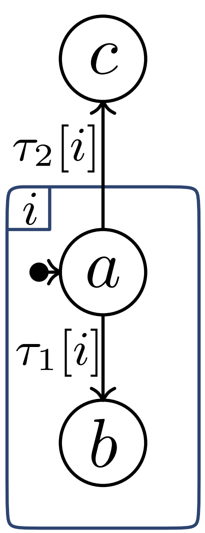
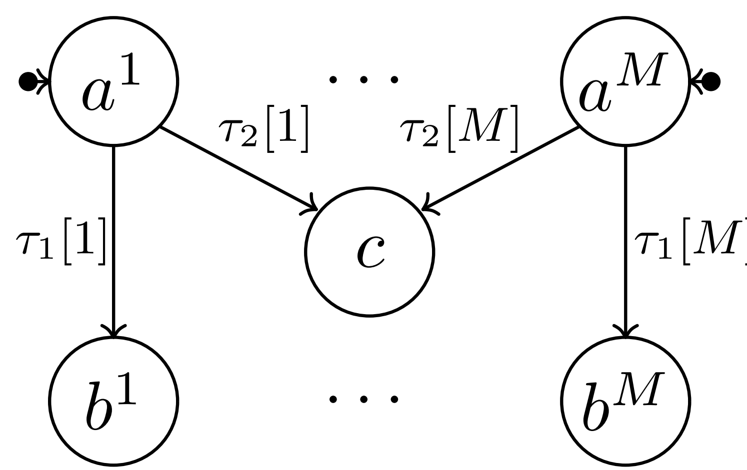


represents $\longrightarrow$



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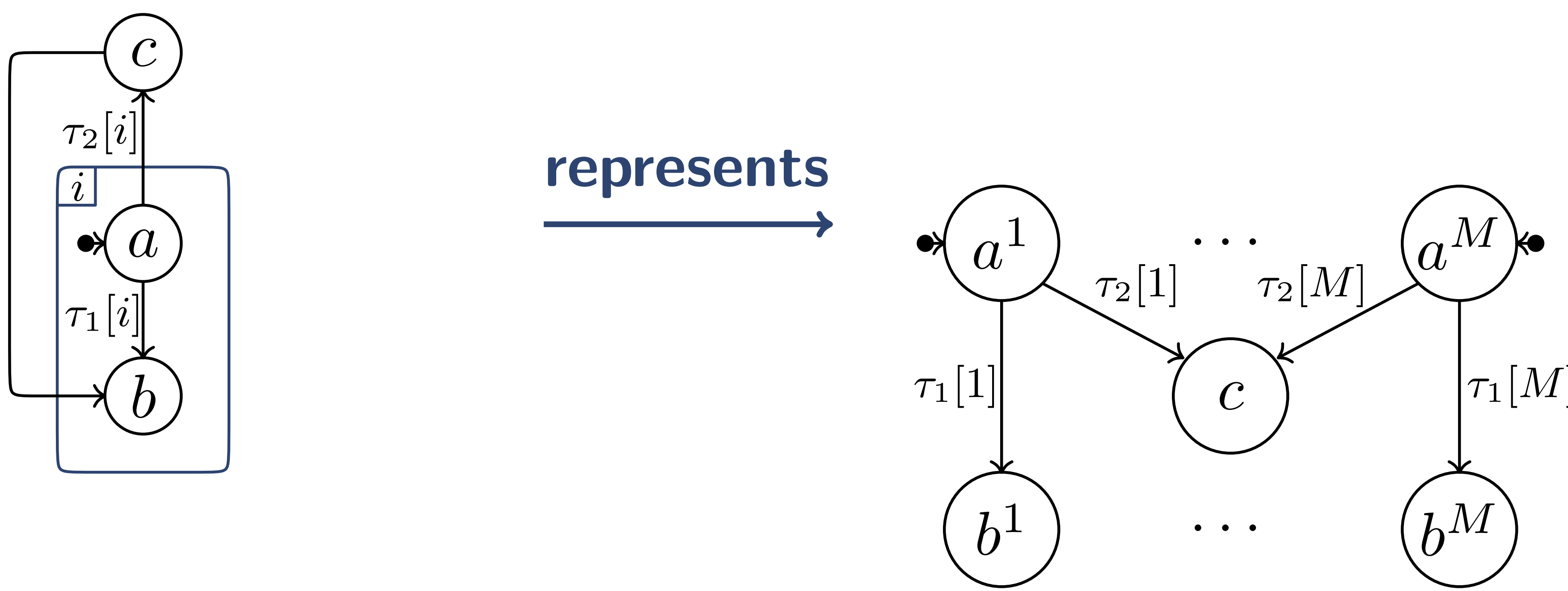

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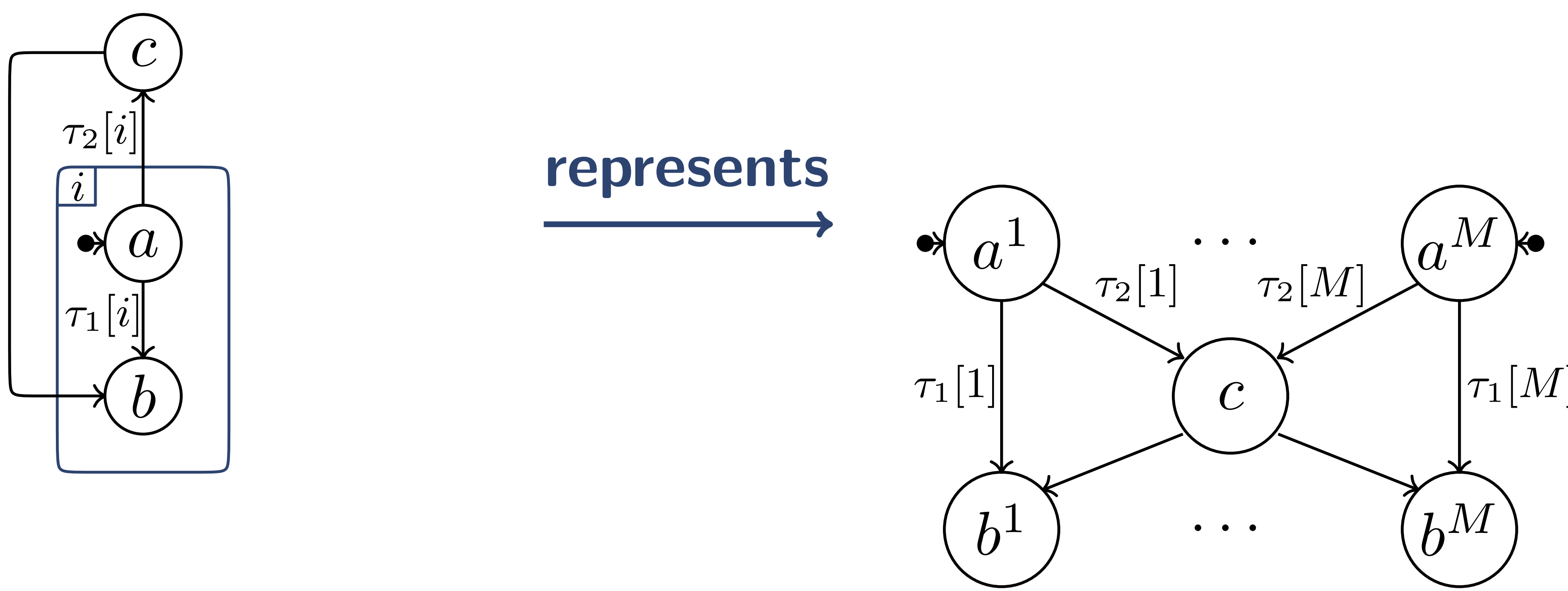

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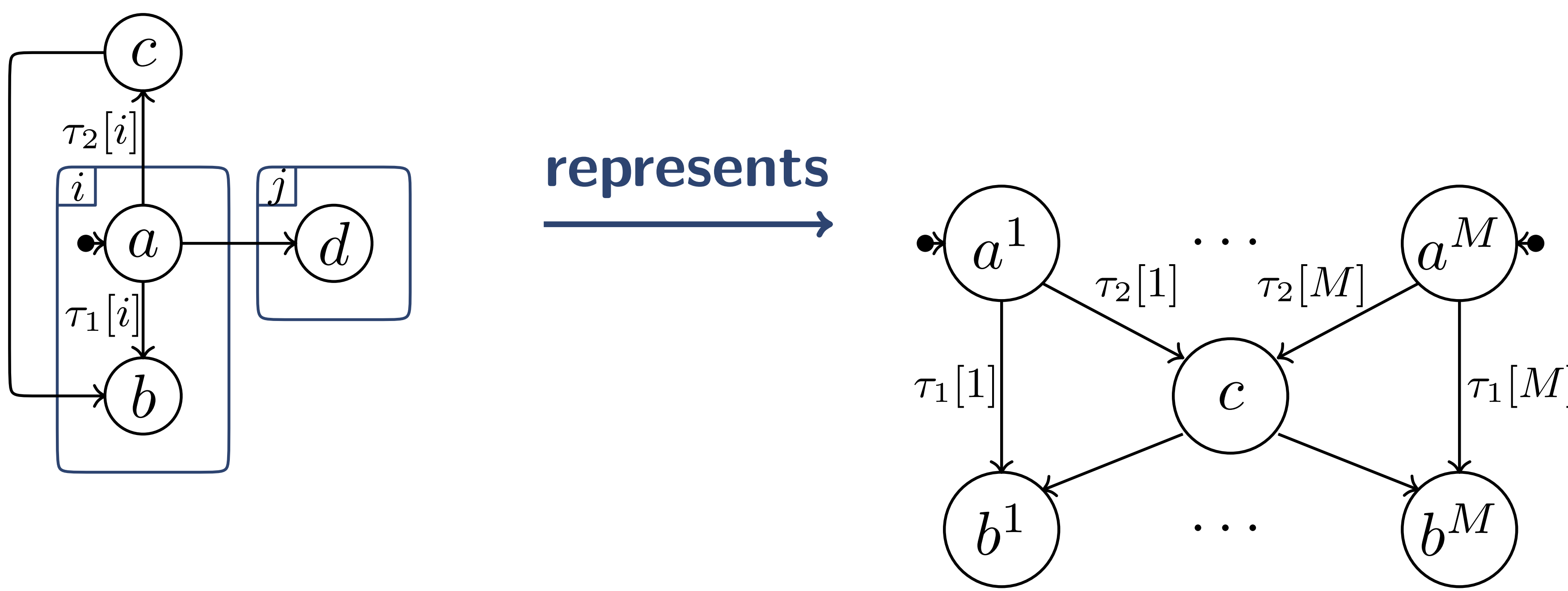

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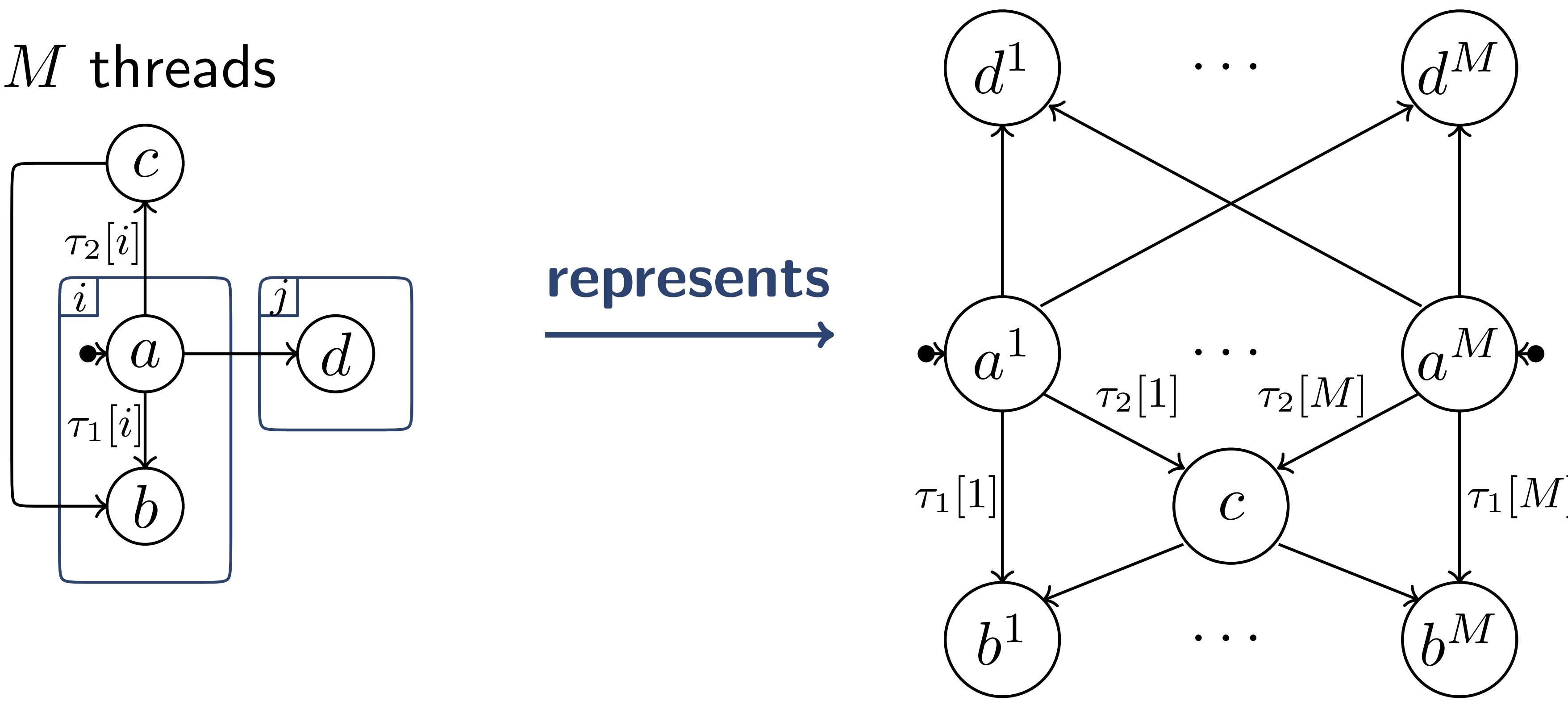

Parametrized Verification Diagrams

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- We add the notion of **boxes**
- A PVD **abstracts all instantiations** of a parametric system

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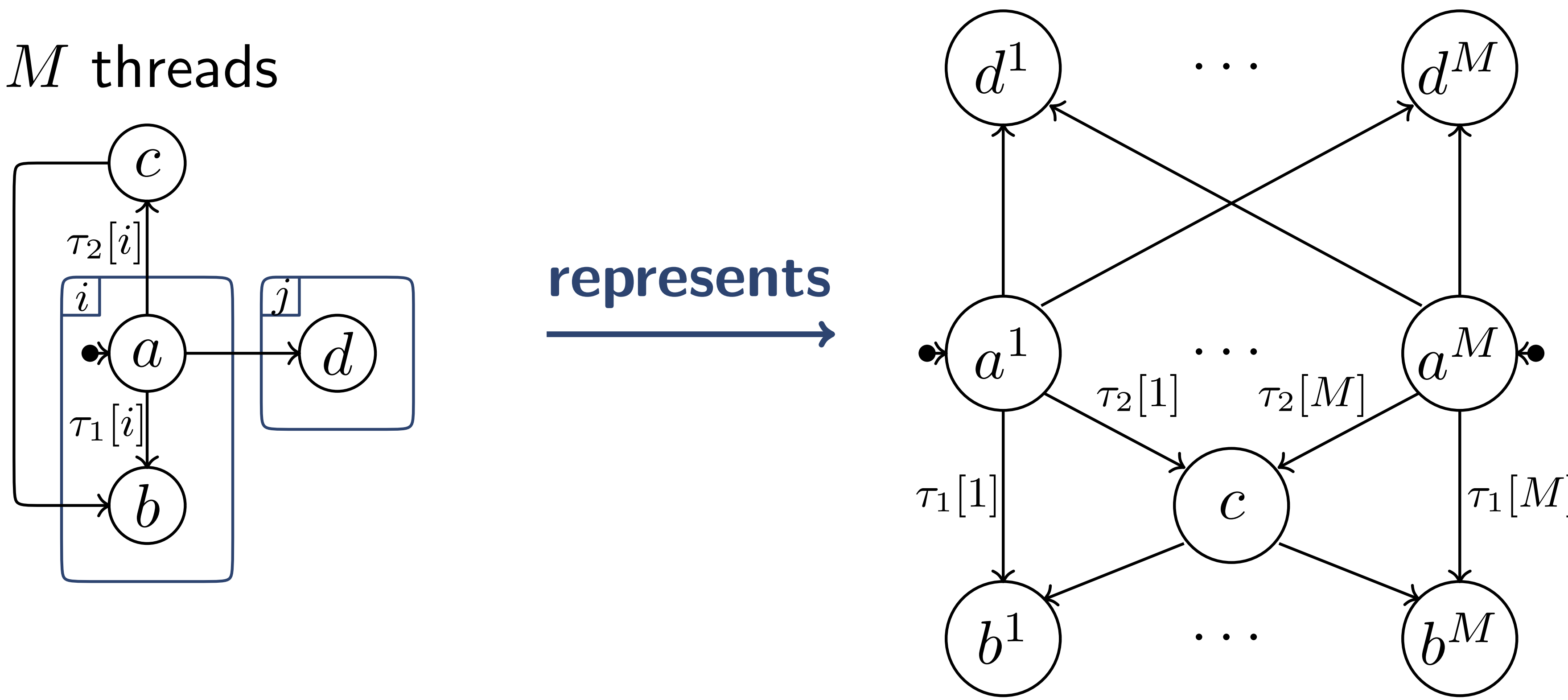

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only tid appearing in n and $succ(n)$ are relevant

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$$\boxed{\begin{array}{lll} \bigwedge_l & n \wedge \tau_l[i_1] & \to succ(n) \\ & \vdots & \vdots \\ \bigwedge_l & n \wedge \tau_l[i_q] & \to succ(n) \end{array}}$$

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 & \vdots & \vdots \\
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\bigwedge_l & n \wedge \tau_l[i] \quad \wedge \quad \bigwedge_{j \in I} i \neq j & \to succ(n)
\end{array}$$

abstracts all other cases thanks to **symmetry**

Verification Conditions for Parametrized Diagrams

- **Initialization:** $\Theta \rightarrow \mu(N_0)$
- **Consecution:** For every $n \in N$ and $\tau \in \mathcal{T}$,

$$\boxed{n \wedge \tau \;\rightarrow\; succ(n)}$$

$$\bigwedge_l \bigwedge_i n \wedge \tau_l[i] \;\rightarrow\; succ(n)$$

$$Voc(n, succ(n)) \;=\; \{i_1, \ldots, i_q\} \;=\; I$$

$$\boxed{\begin{array}{llll}
\bigwedge_l & n \wedge \tau_l[i_1] & & \rightarrow succ(n) \\
& \vdots & & \vdots \\
\bigwedge_l & n \wedge \tau_l[i_q] & & \rightarrow succ(n) \\
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\end{array}}$$

unbounded

$\mathbf{L} \times \mathbf{M}$

Before

bounded

$\mathbf{L} \times (\mathbf{q} + \mathbf{1})$

Now

Verification Conditions for Parametrized Diagrams

- **Initialization:** $\Theta \rightarrow \mu(N_0)$
- **Consecution:** For every $n \in N$, let $I = Voc(n, next(n))$,

$$\begin{array}{lllll} \text{(C1)} & \mu(n)(s) & \wedge\ \rho_{\tau[i]}(s,s') & & \rightarrow \mu(next(n))(s') \quad \text{, for each } i \in I \\ \text{(C2)} & \mu(n)(s) & \wedge\ \rho_{\tau[i]}(s,s') & \wedge \quad \bigwedge_{j \in I} i \neq j & \rightarrow \mu(next(n))(s') \end{array}$$

- **Acceptance:** If $(n_1, n_2) \in P \setminus R$, let $I = Voc(n_1, n_2)$,

$$\text{(a)} \quad \left[\begin{array}{l} \rho_{\tau[i]}(s,s') \wedge \\ \mu(n_1)(s) \wedge \mu(n_2)(s') \end{array} \right] \rightarrow \delta_{j,n_1}(s) \succeq \delta_{j,n_2}(s') \quad \text{, for each } i \in I$$

$$\text{(b)} \quad \left[\begin{array}{l} \rho_{\tau[i]}(s,s') \wedge \bigwedge_{j \in I} i \neq j \quad \wedge \\ \mu(n_1)(s) \wedge \mu(n_2)(s') \end{array} \right] \rightarrow \delta_{j,n_1}(s) \succeq \delta_{j,n_2}(s')$$

and if $(n_1, n_2) \notin P \cup R$,

$$\text{(a)} \quad \left[\begin{array}{l} \rho_{\tau[i]}(s,s') \wedge \\ \mu(n_1)(s) \wedge \mu(n_2)(s') \end{array} \right] \rightarrow \delta_{j,n_1}(s) \succ \delta_{j,n_2}(s') \quad \text{, for each } i \in I$$

$$\text{(b)} \quad \left[\begin{array}{l} \rho_{\tau[i]}(s,s') \wedge \bigwedge_{j \in I} i \neq j \quad \wedge \\ \mu(n_1)(s) \wedge \mu(n_2)(s') \end{array} \right] \rightarrow \delta_{j,n_1}(s) \succ \delta_{j,n_2}(s')$$

- **Fairness:** For each $e = (n_1, n_2) \in E$ and $i \in \beta_v(n_1)$:

$$\begin{array}{lll} \text{(F1)} & \mu(n_1)(s) \wedge \tau[i] \in \eta(e) & \rightarrow En(\tau[i]) \\ \text{(F2)} & \mu(n_1)(s) \wedge \tau[i] \in \eta(e) \wedge \rho_{\tau[i]}(s,s') & \rightarrow \mu(\tau[i](n_1))(s') \end{array}$$

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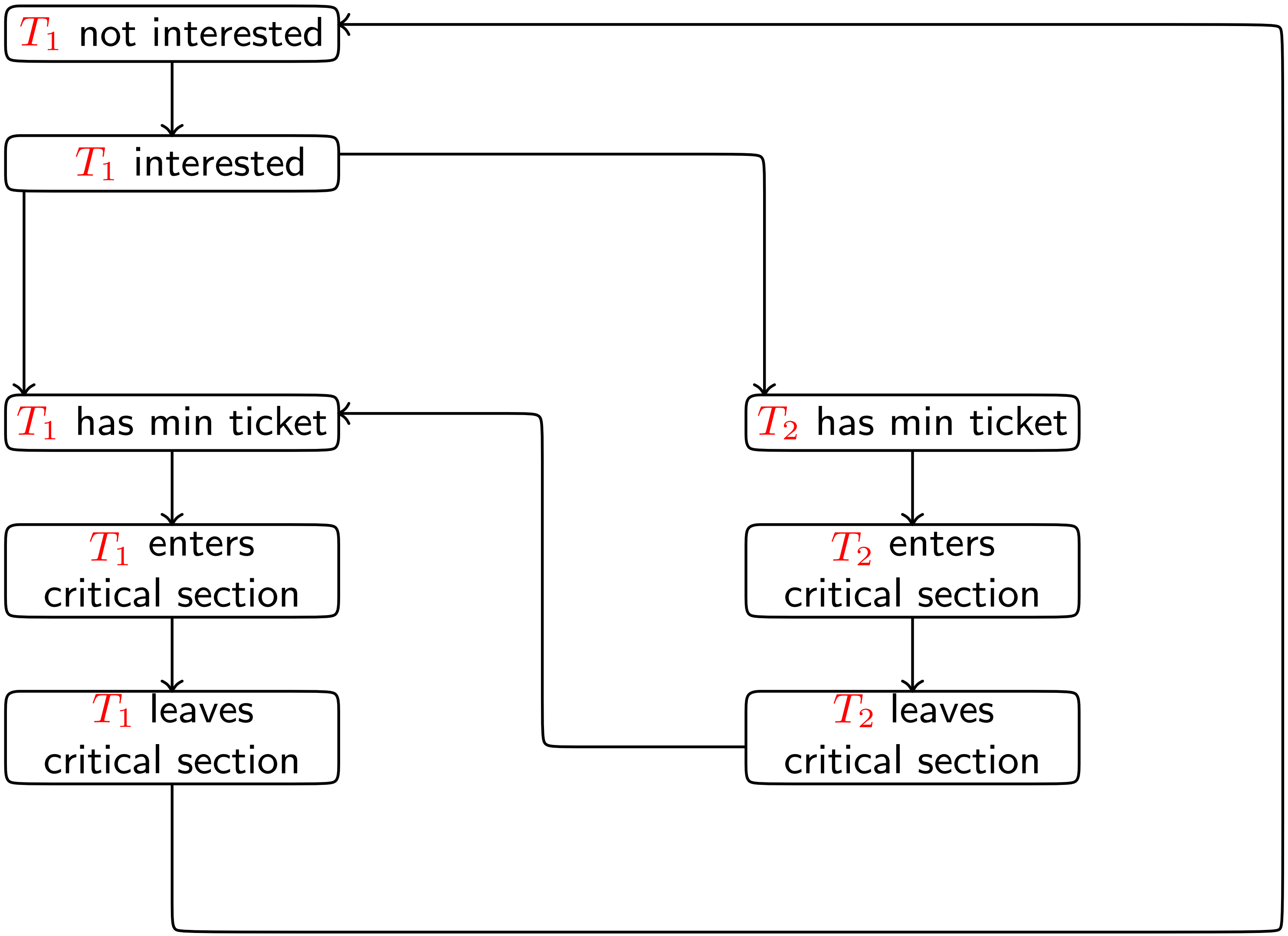

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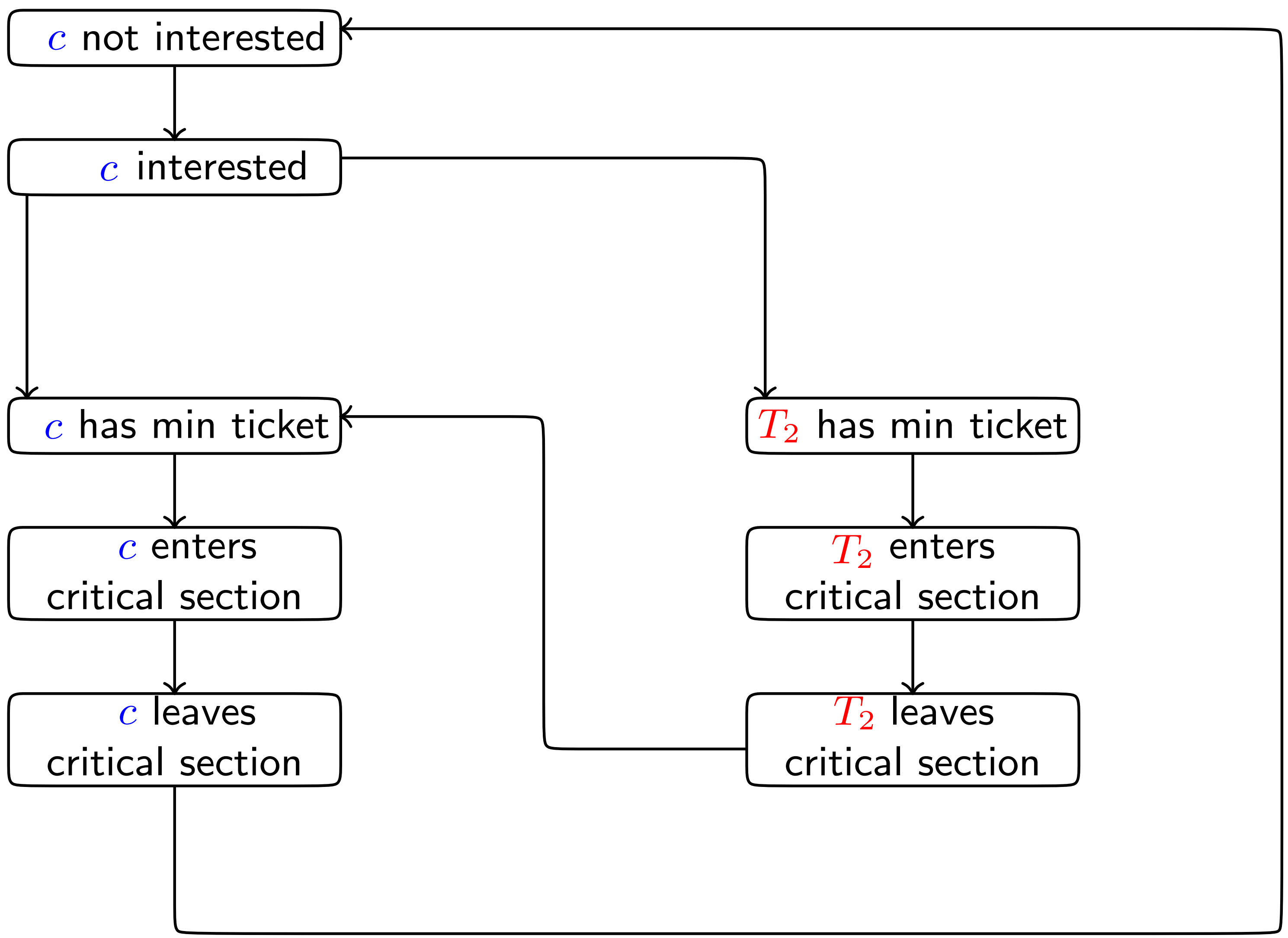

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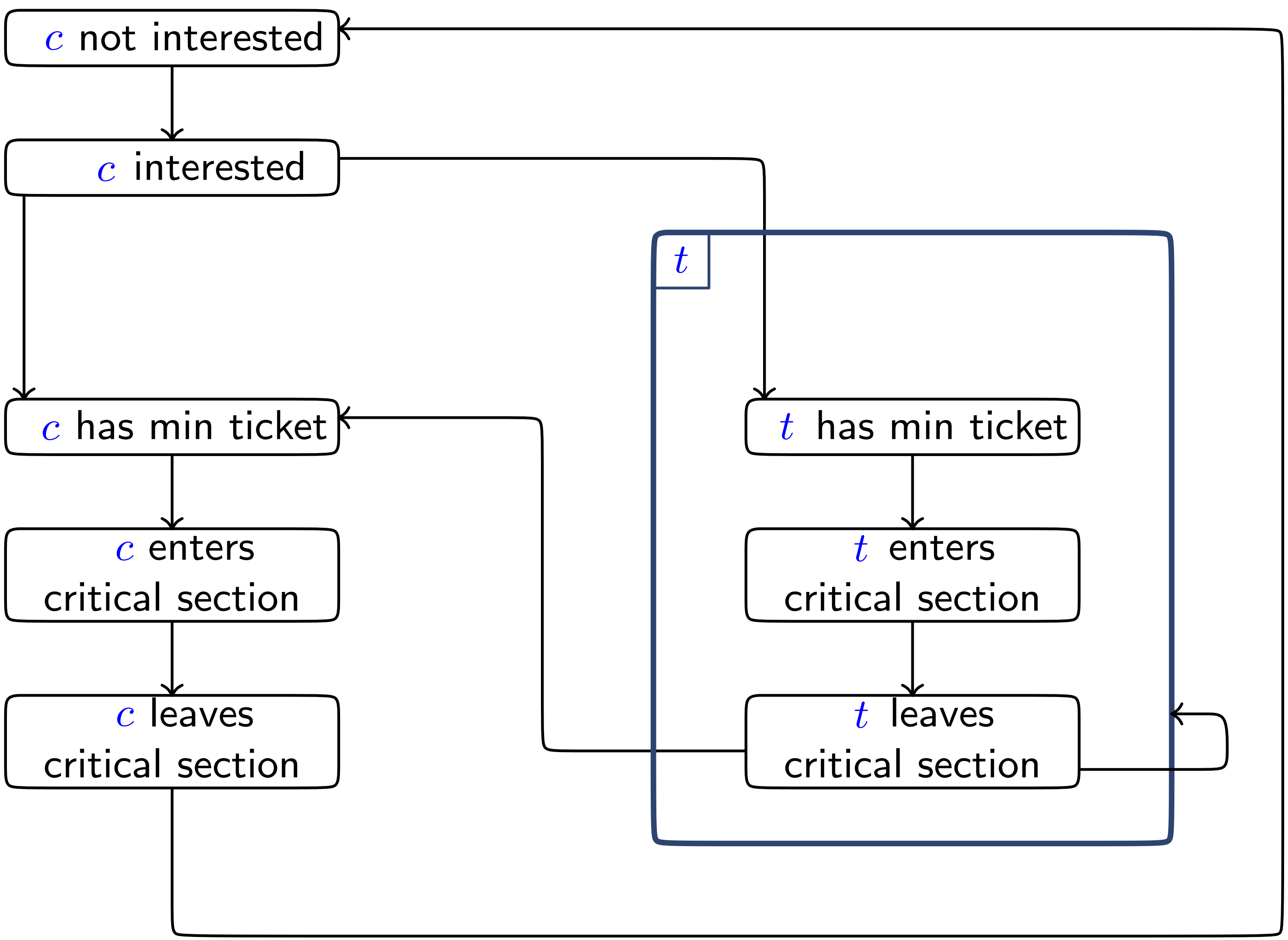

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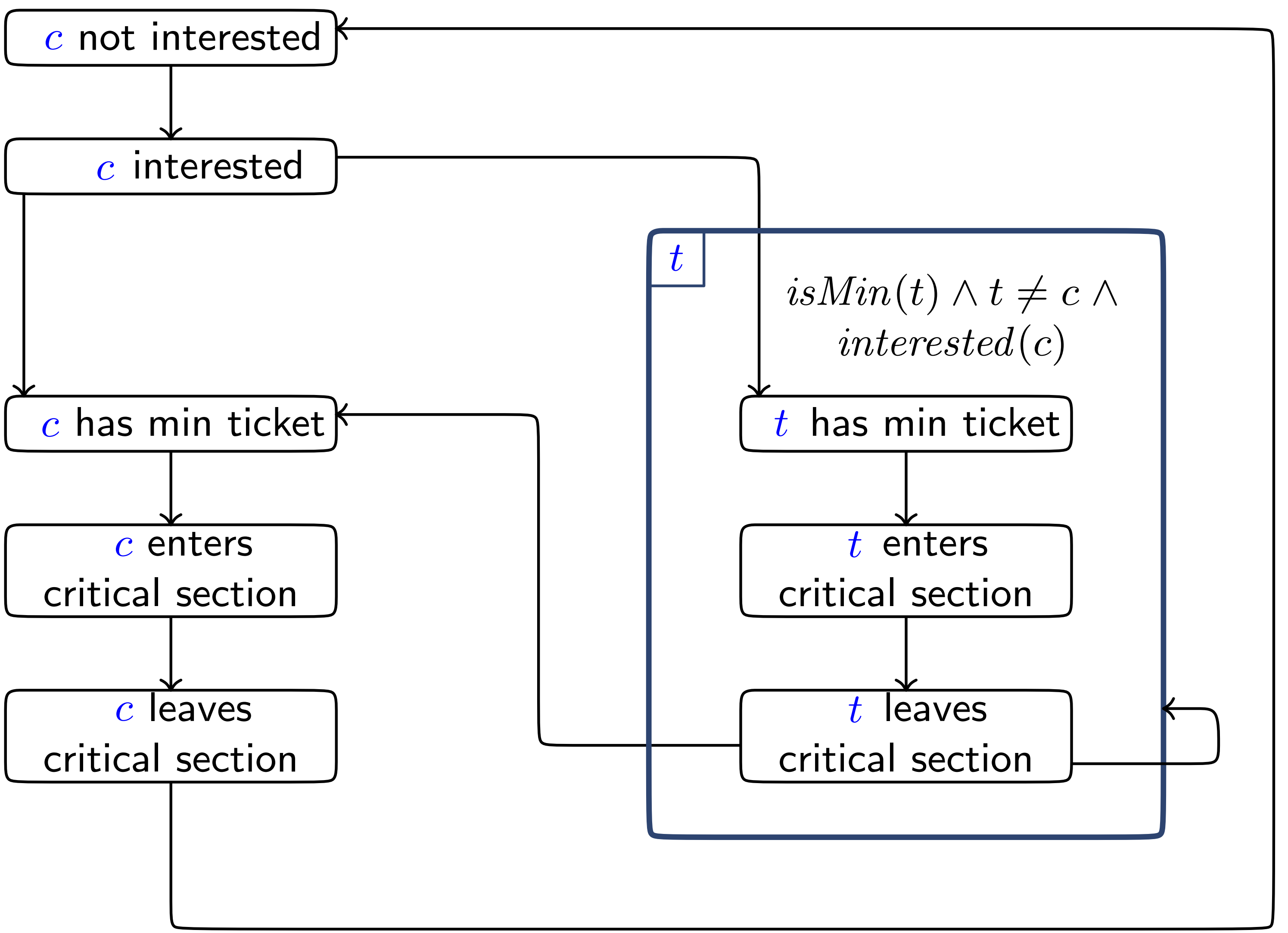

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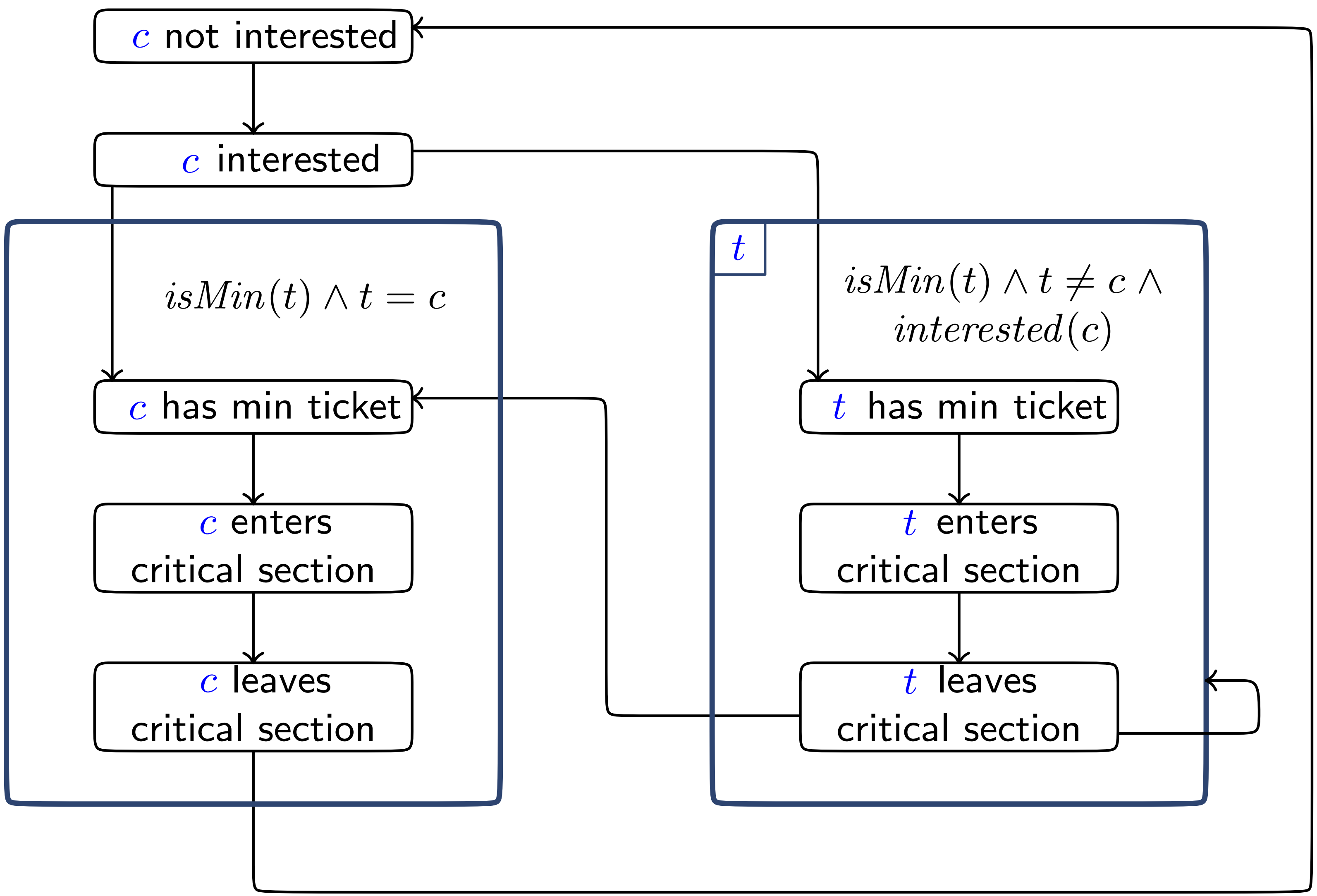

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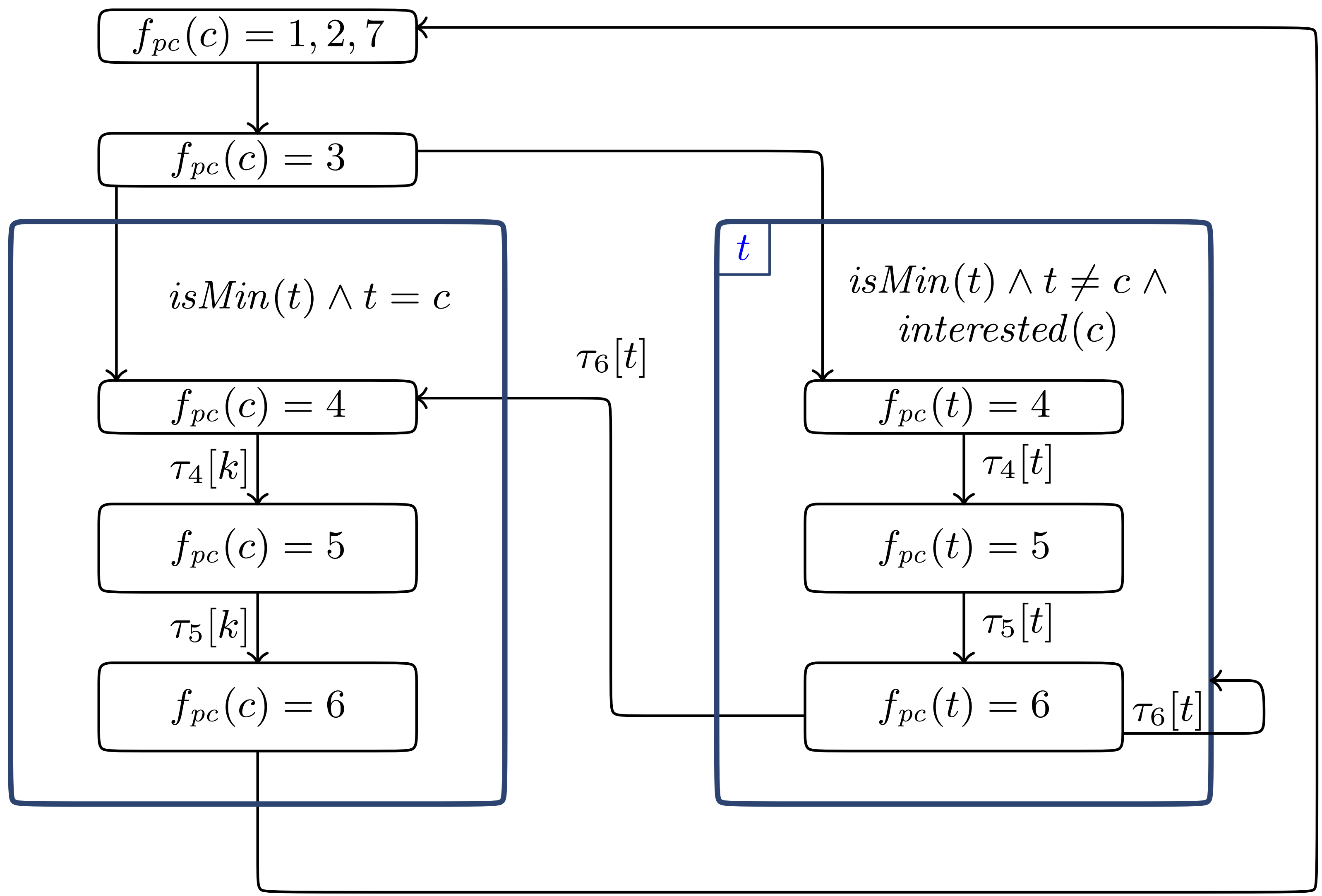

Conclusions

- Sound deductive method for concurrent **parametric systems**
- By now, works over **symmetric systems**
- A **unique diagram** for any arbitrary number of threads
- Proofs based on a **finite number** of **verification conditions**
- Posiblility of **combination** with **decision procedures**
- **Current and future** work:
  - Use of parametrized diagrams for the verification of concurrent list, skiplists, hashmaps...
  - Nested parametrized verification diagrams
  - Extension for non symmetric systems